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Examiner: Sung H Pak
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STATEMENT OF THE CLAIMS

1 - 32 (cancelled)

33. (currently amended) A sigma-delta-type analog-to-digital converter comprising:

~~at least one of~~

an integration stage comprising a resistor, a first heterojunction thyristor device ~~providing high gain amplification~~, and a feedback capacitor, wherein said first heterojunction thyristor has an input terminal and an output terminal, said input terminal operably coupled to said resistor, said feedback capacitor operably coupled between said input terminal and said output terminal, and said first heterojunction thyristor providing high gain amplification of an electrical signal communicated between said input terminal and said output terminal; and

a second heterojunction thyristor device adapted to contemporaneously perform 1-bit analog-to-digital conversion and electrical-to-optical conversion of the result of the 1-bit analog-to-digital conversion.

34. (original) A sigma-delta-type analog-to-digital converter according to claim 33, wherein:

said first heterojunction thyristor device includes a injector terminal electrically coupled to a quantum well channel, a bias current source operably coupled to said injector terminal to provide a desired switching voltage having high gain characteristics,

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and bias resistance that sets a bias current through said first heterojunction device at a point corresponding to said desired switching voltage.

35. (original) A sigma-delta-type analog-to-digital converter according to claim 33, further comprising:

a current source and a third heterojunction transistor that operate in response to a sampling clock signal supplied thereto to reset said second heterojunction thyristor when a sampling period defined by said sampling clock signal has ended.

36. (original) A sigma-delta-type analog-to-digital converter according to claim 35, wherein:

said sampling clock signal comprises one of an electrical clock signal and optical clock signal.

37. (original) A sigma-delta-type analog-to-digital converter according to claim 33, further comprising:

another heterojunction thyristor adapted to operated as a 1-bit DAC in accordance with an output signal produced by said second heterojunction thyristor.

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38. (original) A sigma-delta-type analog-to-digital converter according to claim 37,

wherein:

said output signal comprises one of an electrical signal and optical signal representing results of said 1-bit analog-to-digital conversion performed by said second heterojunction thyristor.

39. (original) A sigma-delta-type analog-to-digital converter according to claim 33,

further comprising:

a decimation circuit operably coupled to electrical output of said second heterojunction thyristor device.

40. (original) A sigma-delta-type analog-to-digital converter according to claim 33,

wherein:

all of said electronic and optoelectronic circuit elements that realize said sigma-delta converter are formed from a common inversion quantum-well channel device structure.